Table # 59: SPI Port-SPI_RDY Timing			
		VDD_EXT 1.8V/3.3V Nominal	
Parameter	Description	Minimum Specification per Rev 0 datasheet	Minimum Specification per Rev A datasheet
		From:	To:
$t_{SRDYSCKM1}$	Minimum Setup time for SPI_RDY De-assertion in Master Mode Before Last SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 1	$(1.5 + BAUD^{1}) \times t_{SCLK0} + 14.5$ ns	$(2.5 + BAUD^{1}) \times t_{SCLK0} + 14.5$ ns